L Number	Hits	Search Text	DB	Time stamp
6	2428	semiconductor with ((wafer workpiece substrate) with rough$4)	USPAT; US-PGPUB; EPO; JPO	2004/11/08 09:18
7	1260	(semiconductor with ((wafer workpiece substrate) with rough$4)) and (die chip 'ic' integrat$3 near3 circuit)	USPAT; US-PGPUB; EPO; JPO	2004/11/08 09:20
8	1213	((semiconductor with ((wafer workpiece substrate) with rough$4)) and (die chip 'ic' integrat$3 near3 circuit)) and surface	USPAT; US-PGPUB; EPO; JPO	2004/11/08 08:51
9	894	(((semiconductor with ((wafer workpiece substrate) with rough$4)) and (die chip 'ic' integrat$3 near3 circuit)) and surface) and (surface with (upper top active back backside bottom))	USPAT; US-PGPUB; EPO; JPO	2004/11/08 09:20
10	8	((((semiconductor with ((wafer workpiece substrate) with rough$4)) and (die chip 'ic' integrat$3 near3 circuit)) and surface) and (surface with (upper top active back backside bottom))) and (rough$4 near3 factor)	USPAT; US-PGPUB; EPO; JPO	2004/11/08 08:59
11	2449	semiconductor with ((wafer workpiece substrate) with rough$4 roughness adj factor)	USPAT; US-PGPUB; EPO; JPO	2004/11/08 09:19
12	384	(semiconductor with ((wafer workpiece substrate) with rough$4 roughness adj factor)) and packag$3	USPAT; US-PGPUB; EPO; JPO	2004/11/08 09:36
13	361	((semiconductor with ((wafer workpiece substrate) with rough$4 roughness adj factor)) and packag$3) and (die chip 'ic' integrat$3 near3 circuit)	USPAT; US-PGPUB; EPO; JPO	2004/11/08 09:20
14	296	(((semiconductor with ((wafer workpiece substrate) with rough$4 roughness adj factor)) and packag$3) and (die chip 'ic' integrat$3 near3 circuit)) and (surface with (upper top active back backside bottom))	USPAT; US-PGPUB; EPO; JPO	2004/11/08 09:20
15	48	roughness adj factor and packag$3	USPAT; US-PGPUB; EPO; JPO	2004/11/08 09:37